Impact de la technologie sur le bruit en 1/f dans les transistors

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Résumé :
La technologie de fabrication des transistors conventionnels MOS utilisant du silicium orienté (100) est si avancée et si bon marché que les groupes leaders en électronique préfèrent développer toujours un peu plus la technologie dans le but de réduire les dimensions des dispositifs électroniques. Il leur faut alors s'adapter à des problèmes technologiques comme les variations de la tension de seuil, l'augmentation du niveau de bruit en 1/f qui est un des problèmes cruciaux des circuits analogiques... Notre but est donc de développer un transistor présentant des performances meilleures que le MOS conventionnel tout en en réduisant le bruit basse fréquence.
Le silicium orienté (100) a été remplacé dans nos transistors par du silicium orienté (110) dans lequel la mobilité des porteurs du canal p est 2.5 fois supérieure à celle trouvée avec l'orientation habituelle. Il en résulte donc une augmentation du courant et par conséquence une fréquence de travail accrue. Malheureusement, ces transistors présentent un niveau de bruit trop important par rapport à celui du transistor à canal p basé sur du silicium (100). Nous avons donc mis en place un nouveau processus de nettoyage de la surface avant la fabrication de la grille n'utilisant pas de solution alkaline qui a eu pour conséquence une baisse de la micro-rugosité de l'interface ainsi qu'une baisse du bruit en 1/f. La différence de bruit entre les deux orientations a été réduite, ce qui laisse bon espoir pour la technologie silicium (110) CMOS.

Abstract :
The technology of common MOSFET based on (100) oriented silicon is now so low cost and so far ahead that world leading microelectronic manufacturers, because of a current low technological cost, prefer follow the incessant demand for fast devices by always developing a step more technology in order to reduce the size of the devices. They have to adapt to technological problems such as V_{th} variation, 1/f noise which is one of the crucial problem for analogue devices, and so on.

Since the current drivability of p-MOS on an Si(110) surface is 3 times larger than that achievable on an Si(100) surface, the (110) CMOS can be considered as a viable competitor or even a future replacement for the current silicon CMOS technology, but, despite this promising feature, with current fabrication techniques, the 1/f noise is still too high for the (110) CMOS to replace the conventional (100) one.

In this paper, we report improvements in device fabrication such as cleaning and oxidation techniques that resulted in a general reduction in noise for both surface orientations. Notably the noise reduction was far more pronounced for the (110) surface, thereby closing the divide between the (110) and (100) p-MOS, bringing a step ahead the (110) technology in the race to achieve ultra-low noise devices.

Introduction :
Low frequency electronic Flicker noise, or 1/f noise, has always been a limiting factor for electronic devices and especially for analog one. If the signal to be transmitted or received is too small it will be shrouded in the device noise. Its reduction or even its hypothetical eradication could lead electronic word into a new era of ultra-low power consumption devices.
The work frequency is, with the 1/f noise, one of the most important parameters we have to take into account for the elaboration of new devices. With a hole current drivability 3 times larger than

the one achieved on Si(100) surface [1, 2], the CMOS technology based on Si(110) presents a 1/f noise level still too high to think about it as a viable competitor or even a replacement for the present (100) CMOS technology as long as the common fabrication techniques will be applied. In this paper, we report improvements in device fabrication that resulted in a general reduction in noise for both surface orientations. Notably the noise reduction is far more pronounced for the (110) surface, thereby closing the divide between the (110) and (100) p-MOS in the race to achieve ultra-low noise devices. These improvements are attributed to the use of an alkali-free 5 steps room temperature cleaning process [3, 4], which reduces surface micro-roughness, combined with microwave-excited high-density plasma oxidation technology [5] giving a more uniform high quality silicon-silicon oxide interface.

Experimental :

A 5 nm thick gate oxide has been formed using a microwave-excited high-density plasma oxidation at 400°C as well as a thermal oxidation at 900°C. Previously to this, Si(110) and Si(100) surfaces have been prepared for the gate oxidation formation using both RCA and the alkali-free 5 steps room temperature cleaning [4]. Every p-MOS presented 1/f noise which has been measured

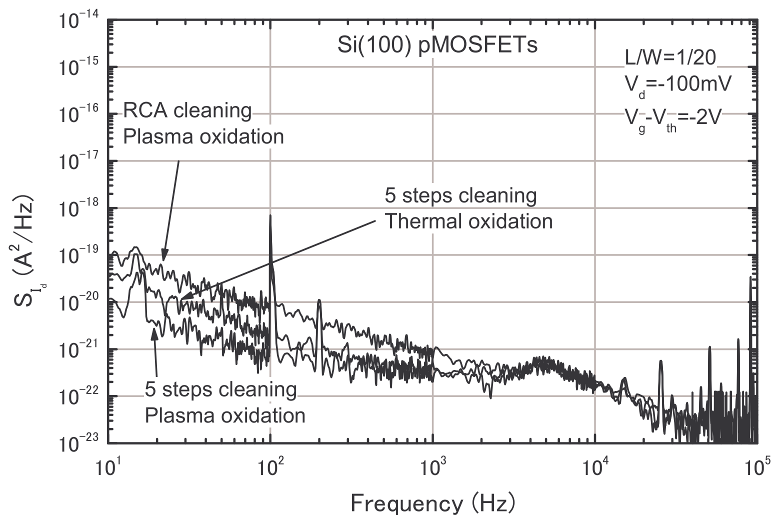

FIGURE 1. Evolution of the spectral density of drain current in a (100) silicon surface oriented pMOS for two different cleaning processes and two different oxidation techniques.

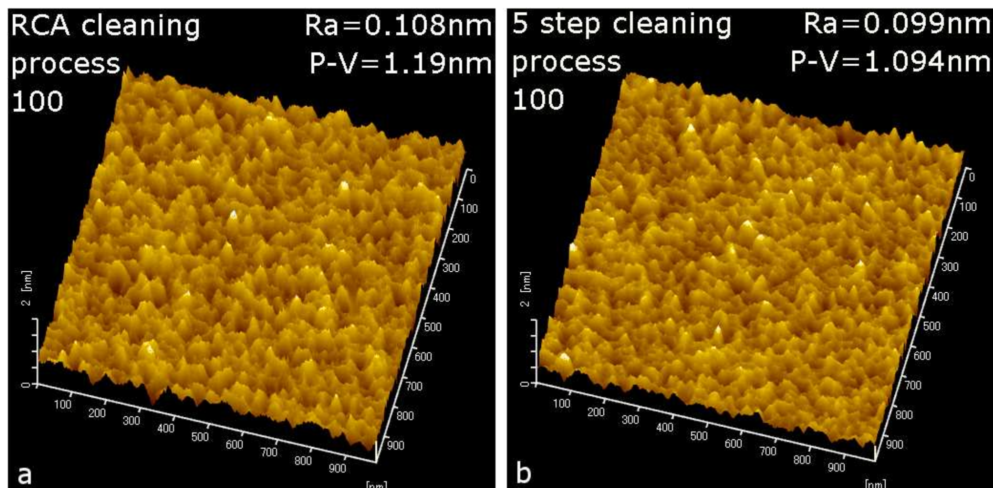

FIGURE 2. Micro-roughness Ra and peak-valley maximum amplitude P-V with the RCA cleaning (a) and the 5 step cleaning (b) for (100) silicon oriented surface (2x1000x1000nm).

with a vector Signal Analyzer (89410A AGILENT) directly on wafer biased by an Ultra-Low DC Source (PA14A1 SHIBASOKU).

Results and discussion :

Typical results of electronic noise measurement on (100) p-MOS are shown in figure 1. Several evaluations were made for all combinations of cleaning and oxidation procedures. The oxidation process has a pronounced impact on low frequency noise, giving plasma oxidation preference over the thermally induced one. The cleaning process has also a pronounced impact on the 1/f noise level, which decreases by almost one decade when using the alkali-free 5 steps cleaning. Actually, this can be explained by the quality of surface before oxidation as presented on figure 2 with the STM images of Si(100) surfaces processed respectively with the conventional RCA cleaning and the alkali-free 5 steps cleaning. The improvement in surface quality when alkali-free 5 steps cleaning used corresponds to a reduction in the peak-valley height and average micro-roughness (Ra) found to be around 10%. Numerous steps and high temperature are used in RCA cleaning. Furthermore it requires the use of alkaline solution which leads to anisotropic removal of silicon atoms from the surface. In fact, the alkaline solution, by bond cleavage, leads to the formation of micro-structured

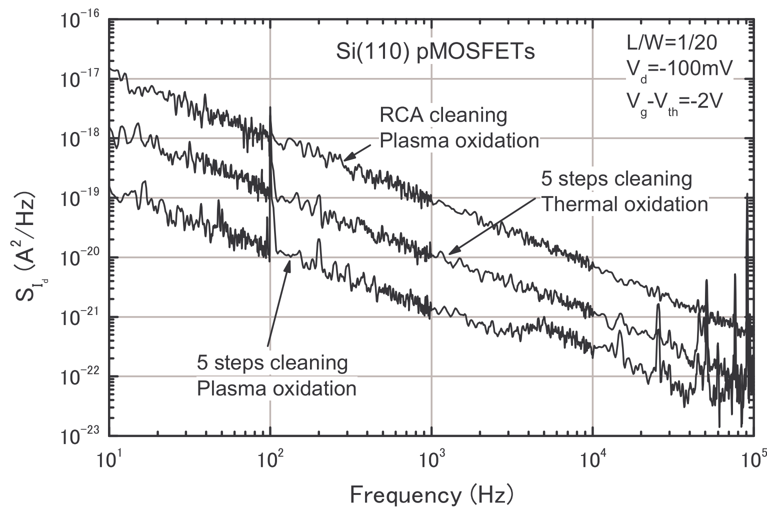

FIGURE 3. Evolution of the spectral density of drain current in a (110) silicon surface oriented pMOS for two different cleaning process and two different oxidation technique.

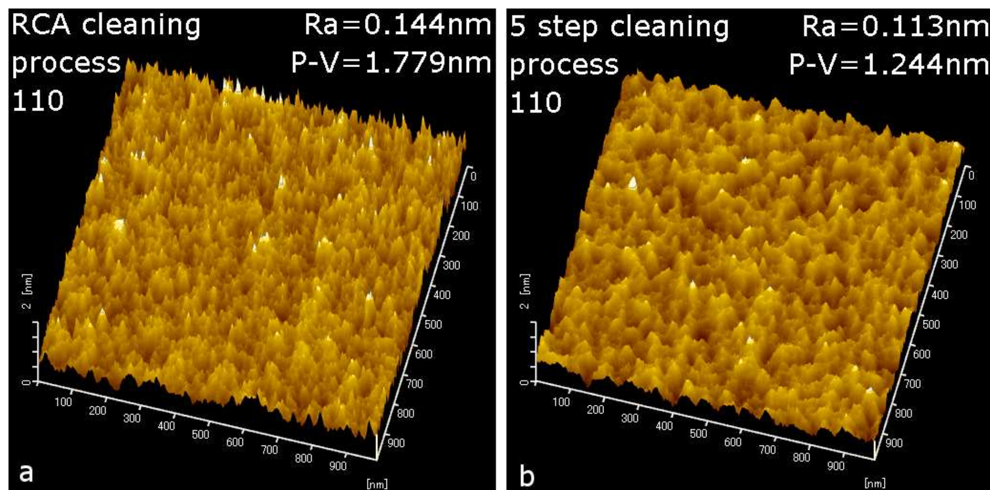

FIGURE 4. Micro-roughness Ra and peak-valley maximum amplitude P-V with the RCA cleaning (a) and the 5 step cleaning (b) for (110) silicon oriented surface (2x1000x1000nm).

inhomogeneities oriented (111) all over the treated surface. These local micro-structures are building up over time and can even be visible to naked eye if silicon atoms are sufficiently exposed. On the contrary, the 5 steps cleaning process is alkali-free resulting in the formation of a smoother, homogeneous silicon-oxide interface. With an oxidation rate regardless to the orientation of the micro-surface upon which it acts [6], the plasma oxidation builds with time a smoother and more uniform Si-SiO_2 interface. Because of an oxidation rate slower on Si(100) surfaces than that on Si(110) or Si(111), thermally induced oxide will present a rougher interface and thickness inhomogeneities along channel.

The same procedure described above has been carried out on Si(110) p-MOS. Looking at the results of 1/f noise measurements shown in figure 3 and at the STM images presented on figure 4 and when compared to those obtained for the conventional orientation, we assist to a larger reduction of low frequency noise and a better improvement of the micro-roughness by once more simply changing the pre-gate formation cleaning to the 5 steps cleaning. The cleaning process has an impact much more pronounced on Si(110) than on Si(100). The degradation of the surface resulting from RCA cleaning shown in figure 4a which is far worse compared to that shown in figure 2a can be explained by the fact that the alkali solution etching rate on Si(110) is faster than on Si(100) [7]. This significant change in the noise level has its origin in the cleaning process and the resulting surface quality of the Si-SiO_2 interface and in particular the change in the micro-surface roughness.

This can be attributed to the faster degradation of the Si(110) surface caused by the alkaline solution used during RCA cleaning compared to the degradation of the Si(100) surface under the same conditions. Thus the choice of cleaning method can have a knock-on effect which may be amplified during the gate formation step and this will be especially true in the case of thermal oxidation.

Conclusion :

Dependence of the surface micro-roughness on the 1/f noise in p-MOS has been studied. We successfully demonstrated that the use of an alkali-free cleaning for a reduction of the micro-roughness and its combination with a plasma process for the realization of the gate oxide lead to a significant suppress in the 1/f noise level due to the formation of a smoother interface and more uniform oxide growth. The advantage of the (100) p-MOS over the (110) p-MOS has been reduced so much that, considering the drivability of (110) p-MOS, the (110) CMOS will be soon able to establish itself as a viable competitor for the current silicon CMOS technology.

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